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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 02/03/2009

Roger Fulghum
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910 Louisiana Street
Houston, TX 77002-4995

EXAMINER	
AHMED, HAMDY S	
ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/03/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,427	08/20/2003	Gary J. Verdun	016295.1422	7003

TITLE OF INVENTION: SYSTEM AND METHOD FOR MANAGING POWER CONSUMPTION AND DATA INTEGRITY IN A COMPUTER SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	05/04/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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One Shell Plaza
910 Louisiana Street
Houston, TX 77002-4995

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

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10/644,427	08/20/2003	Gary J. Verdun	016295.1422	7003

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nonprovisional	NO	$1510	$300	$0	$1810	05/04/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
AHMED, HAMDY S	2188	711-133000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 611 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 611 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/644,427	VERDUN, GARY J.	
	Examiner	Art Unit	
	HAMDY S. AHMED	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *01/15/2009*.

2. ☒ The allowed claim(s) is/are *1, 2, and 4-23*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

Claim 3, is cancelled.

Claims 1-2, and 4-23 are allowed.

The following is the examiner's statement of allowance:

With respect to claim 1, the limitations of "… a computer system, comprising: a processor; a cache associated with the processor; a system memory; a memory controller hub that is operable to track writes to the system memory by one or more bus masters operable to access the .system memory; a write tracking buffer external to the processor, wherein the write tracking buffer is communicatively coupled to the cache via the processor and to the system memory", are well known. But the prior art of record, specifically Schuckle et al (US No: 7,017,054 B2), taken either individually or combination fails to teach or suggest the limitation in combination of"… and wherein the write tracking buffer is operable to hold as entries the addresses of one or more writes to the system memory made during a period that the .processor is in a low power state; wherein the memory controller hub is operable to: initialize the write tracking buffer when the processor enters a low power state identify one or more writes to the system memory made during the period that the processor is in the low power state; determine if the write tracking buffer is full during the period that the processor is in the low power state; and if the write tracking buffer is not full, record the addresses of the one or more writes; and wherein the processor is operable to write to the system memory one or more lines of cache prior to the processor entering its low power state, and wherein the processor is operable to invalidate one or more lines of cache corresponding to the entries of the write tracking buffer upon the processor exiting its low power state"

With respect to claim 5, the limitations of "… a method for managing the power

consumption by a processor in a computer system, the computer system including a system memory and the processor including an internal cache, comprising the steps of: maintaining a buffer in a memory controller hub that is operable to track one ore more writes to the system memory by one or more bus masters operable to access the system memory, wherein the buffer is: external to the processor; and communicatively coupled to the internal cache via the processor and to the system memory"; are well known. But the prior art of record, specifically Schuckle et al (US No: 7,017,054 B2), taken either individually or combination fails to teach or suggest the limitation in combination of"... causing the processor to enter a low power state; initializing the buffer when the processor enter the low power state; during a period that the processor is in a low power state: identifying one or more writes to the system memory made during the determining if the buffer is full; if the buffer is not full, recording one or more addresses writing in a buffer external to the processor the addresses of modified data in the .system and upon the processor exiting the low power state, invalidating one or more lines in the internal cache that correspond to the memory addresses recorded in the buffer".

With respect to claim 12, the limitations of "... a method for managing cache coherency in an information handling system, the information handling system including a processor with an internal cache and a system memory, comprising the steps of: maintaining a buffer in a memory controller hub that is operable to track one or more writes to the system memory by one or more bus masters operable to access the system memory, wherein the buffer is: external to the processor; and communicatively coupled to the internal cache via the processor and to the system memory; performing a write back operation to write to the system

memory one or more cache lines that have been modified relative to content at corresponding memory addresses in the system memory" are well known ; But the prior art of record, specifically Schuckle et al (US No: 7,017,054 B2), taken either individually or combination fails to teach or suggest the limitation in combination of"... causing the processor to enter a low power state; initializing the buffer when the processor enter the low power state; during a period that the processor is in the low power state: identifying one or more writes to system memory made during the period; determining if the buffer is full; if the buffer is not full, recording memory addresses of data in the system memory that have been modified by a bus master in the information handling system; and upon the processor exiting the low power state for a higher power state, invalidating in the internal cache one or more cache lines corresponding to the memory addresses recorded in the buffer".

With respect to claim 17, the limitations of "... an information handling system, comprising: a processor having an internal processor cache; a system memory; a buffer; a memory controller; wherein the memory controller is operable to populate the buffer with one or more addresses of writes made to the, system memory during a period that the processor is in a low power state, wherein the buffer is: maintained in the memory controller; external to the processor; and communicatively coupled to the internal processor cache via the processor and to the system memory"; are well known. But the prior art of record, specifically Schuckle et al (US No: 7,017,054 B2), taken either individually or combination fails to teach or suggest the limitation in combination of"... wherein the memory controller is operable to: initialize the buffer when the processor enters the low power state; identify one or more writes to the system memory made during the period that the processor is in the low power state; determine if the buffer is full during the period that the processor is in the low power state; and if the buffer is not full, record the addresses of the one or more writes; and wherein the processor, upon entering

the low power state, is operable to write to the system memory one or more lines of cache and, upon exiting the low power state, is operable to invalidate cache lines of the internal .processor cache corresponding to the addresses recorded in the buffer".

With respect to claim 21, the limitations of " a method for managing cache coherency in a computer system following the entry of a processor into a low power state, the computer system including a processor having an internal cache, a system memory, and a write tracking buffer that is external to the processor, is communicatively coupled to the internal cache via the processor and to the system memory, and is operable to store the addresses of system memory addresses modified during a period that the processor was in the low power state, wherein the write tracking buffer is maintained in a memory controller hub that is operable to track one or more writes to the system memory by one or more bus masters operable to access the system memory", are well known. But the prior art of record, specifically Schuckle et al (US No: 7,017,054 B2), taken either individually or combination fails to teach or suggest the limitation in combination of"… comprising the steps of: causing the processor to enter a low power state; initialize the write tracking buffer when the processor enter the low power state; during the period that the processor is in a low power state: identifying one or more writes to the system memory made during the determining if the write tracking buffer is full; if the write tracking buffer is not full, recording one or more memory addresses of modified data in the system memory; causing the processor to exit the low power state; and invalidating in the internal cache those cache lines corresponding to the one or more memory addresses stored in the write tracking buffer".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HAMDY S. AHMED whose telephone number is (571)270-1027. The examiner can normally be reached on M-TR 7:30-5:00pm and Every 2nd Friday 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S. Sough/
Supervisory Patent Examiner, Art Unit 2188
01/30/09

/Hamdy S Ahmed/
Examiner, Art Unit 2188